OIPE DEC 06 2005 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified)	ATTY. DOCKET NO.	SERIAL NO.:
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	IL920030035US1	10/695,970
	APPLICANT: Ben-David et al.	
	FILING DATE: 29-Oct-2003	GROUP: ~~2183~~ 2191

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
MA	AA	**6665790**		Glossner et al.			2000-02-29
MA	AB	**6915411**		Moreno et al.			2002-07-18
MS	AC	**2004-0078554**		Glossner et al.			2003-06-07

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

MA	AD	Preeti Ranjan Panda, Nikil D. Dutt, and Alexandru Nicolau. "Efficient utilization of sratch-pad memory in embedded processor applications", in European Design and Test Conf., March 1997
MA	AE	Keith D. Cooper, Timothy J. Harvey. "Compiler controlled Memory", Eighth Int. Conf. on Architectural Support for Programming Languages and Operating Systems, pp. 100-104, Oct, 1998
MA	AF	Masaaki Kondo, Hideki Okawara, Hiroshi Nakamaru, Taisuke Boku. "SCIMA: Software Controlled Integrated Memory Architecture for High Performance Computing", http://citeseer.nj.nec.com/376639.html
MA	AG	William Y. Chen, Roger Bringmann, Scott A Mahlke, Richard E. Hank, James E. Sicolo. "An Efficient Architecture for Loop Based Data Preloading", 25th Annual International Symposium on Microarchitecture (1992) http://citeseer.nj.nec.com/chen92efficient.html
MA	AH	Matthew A. Postiff, Trevor Mudge. "Smart Register Files for High Performance Microprocessors". http://citeseer.nj.nec.com/postiff99smart.html
MA	AI	Matthew A. Postiff, David Greene, Steve Raasch, Trevor Mudge. "Integrating Superscalar Processor Components to Implement Register Caching". http://citeseer.nj.nec.com/468226.html
MA	AJ	Jesus Corbal, Roger Espasa, and Mateo Valero. "Exploiting a new level of DLP in multimedia applications", in Intl. Symposium on Microarchitecture, pages 72-79, 1999.

EXAMINER M. Thulin DATE CONSIDERED 2·6·2007

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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MH	AK	Huy Nguyen and Lizy Kurian John. "Exploiting SIMD parallelism in DSP and multimedia algorithms using the AltiVec technology", in Intl. Conf. on Supercomputing, pages 11-20 1997
MH	AL	A. J. C. Bik, M. Girkar, P. M. Grey, and X. Tian. "Efficient exploitation of parallelism on Pentium III and Pentium 4 processor-based systems", Intel Technology J., February 2001.
MH	AM	Andreas Krall and Sylvain Lelait. "Compilation techniques for mutimedia processors", Intl. J. of Parallel Programming, 28(4):347-361, 2000.
MH	AN	Samuel Larsen, Emmet Witchel, and Saman Amarasinghe. "Techniques for increasing and detecting memory alignment", Technical Memo 621, MIT LCS, Novermber 2001.
MH	AO	David Callahan et al. "Improving Register Allocation for Subscripted Variables", Proceedings of the ACM SIGPLAN '90 Conference on Programming Language Design and Implementation, White Plains NY, June 20-22, 1990.
MH	AP	Kandemir et al., "Optimizing Inter-Nest Data Locality", CASES 2002, Oct. 8-11 2002, Grenoble, France
MH	AQ	Doshi et al., "Optimizing Software Data Prefetches with Rotating Registers", IEEE 2001, 257-267.

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	2.6.2007

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MH	AR	Jaewook Shin et al., "Compiler-Controlled Caching in Superword Register Files for Multimedia Extension Architectures", in Int. Conf. on Parallel Architectures and Compiler Techniques, pages 45--55, 2002.
MH	AS	Keith Cooper et al., "Cross-loop Reuse Analysis and its Application to Cache Optimizations", Lecture Notes In Computer Science; Vol. 1239 archive Proceedings of the 9th International Workshop on Languages and Compilers for Parallel Computing, Pages: 1-19, 1996

EXAMINER	DATE CONSIDERED
Mary Shelton	2.6.2007

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